

604663 " 3046630

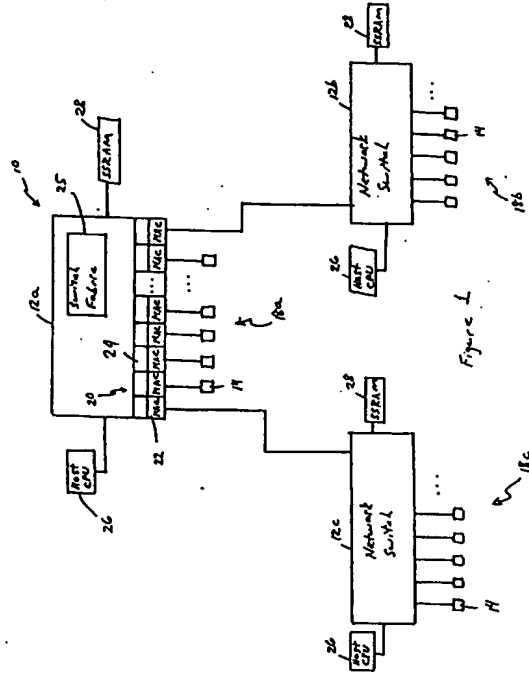


Figure 1

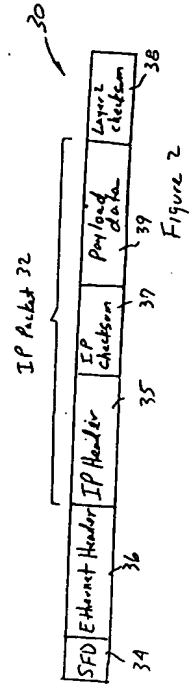


Figure 2

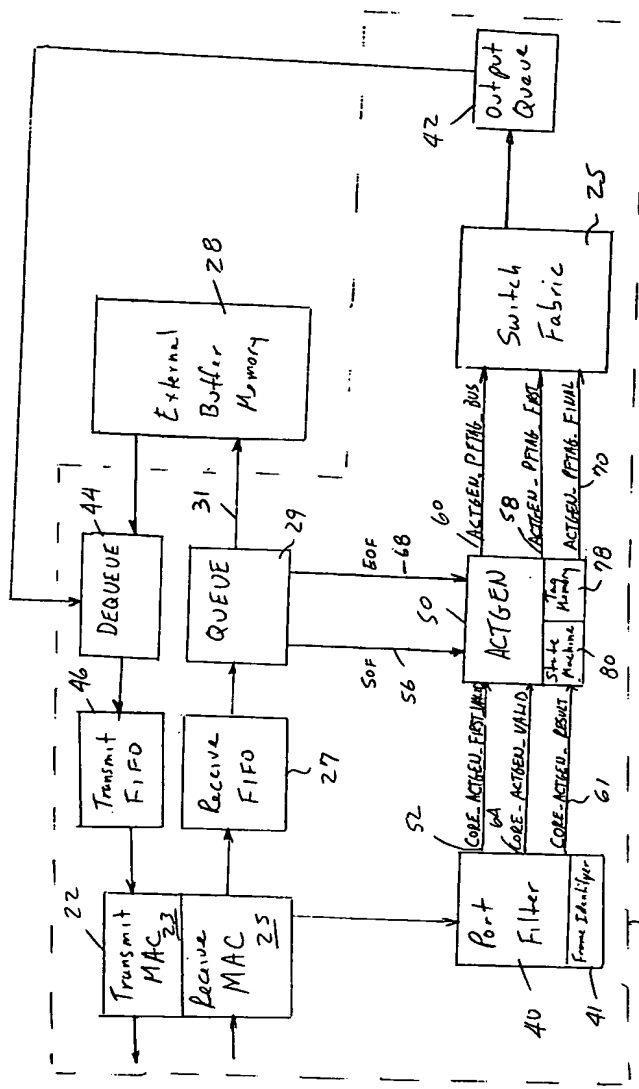


Figure 3

Timing diagram for the first tag result. The diagram shows signals: CORE_ACTGEN_FIRST_VALID (52), FIRST_RESULT_READY (54), MP_MS_RB_STAT[0] (SOF) (56), ACTGEN_PFTAG_FIRST (58), ACTGEN_PFTAG_BUS (60), CORE_ACTGEN_VALID (64), FINAL_RESULT_READY (66), MP_MS_RB_STAT[1] (EOF) (68), and ACTGEN_PFTAG_FINAL (70). It also shows two bus signals: 74 - WR_ADDR (0 then 1) and 76 - RD_ADDR (0 then 1). The diagram is divided into two sections: 'FIRST TAG RESULT' and 'FINAL TAG RESULT'. Arrows indicate data flow and timing relationships between the signals.

Figure 4

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graph TD
    92[RESET] --> 90{Start of frame}
    90 -- N --> 92
    90 -- Y --> 94[START]
    94 --> 96{CORE_ACTGEN_FIRST_VALID  
OR  
FIRST_RESULTS_READY}
    96 -- N --> 94
    96 -- Y --> 98([ACTGEN_PFTAG_FIRST])
    98 --> 100[WAIT_EOF]
    100 --> 102{End of frame}
    102 -- N --> 100
    102 -- Y --> 104[WAIT_FINAL]
    104 --> 106{CORE_ACTGEN_VALID OR  
FINAL_RESULTS_READY}
    106 -- N --> 104
    106 -- Y --> 108([ACTGEN_PFTAG_FINAL])
    108 --> 92

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Figure 5